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| EXAMINER | |
|---|---|
| MONDT, JOHANNES P | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/751,714 | LUK ET AL. | |
| | Examiner | Art Unit | |
| | Johannes P. Mondt | 3663 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *8/13/7, 8/16/7, 10/25/7*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *21-23 and 29-35* is/are withdrawn from consideration.

5)☒ Claim(s) *3-8,17-20,24-28,36 and 37* is/are allowed.

6)☒ Claim(s) *1,2 and 9-15* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

Amendment and Terminal Disclaimer filed 8/13/07, and Amendment filed 10/25/07 submitted upon request by examiner to reflect the correct status of the claims form the basis for this Office Action. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments". Claims 1-37 are in the application, claims 21-23 and 29-35 have been withdrawn following the finality of a restriction / election requirement (see previous office action mailed 5/11/07), claims 3-8, 17-20, 25-28 and 36-37 are allowed.

### *Terminal Disclaimer*

The terminal disclaimer filed on 8/13/07 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of prior patent 7,116,594 has been reviewed and is accepted. The terminal disclaimer has been recorded.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. ***Claim 12*** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use

the invention. In particular, a gate diode otherwise defined by claim 12 with the source diffusion region abutting the gate and drain diffusion region abutting another side of gate wherein the second terminal is coupled to the source diffusion region and wherein the first terminal is coupled to the gate is not AND CANNOT BE a two-terminal semiconductor device but instead a one-terminal semiconductor device, because source/drain and gate are short-circuited.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 1-2, 9-10 and 13-15*** are rejected under 35 U.S.C. 102(b) as being anticipated by Mead et al (5,844,265). With reference to the rejection above under 35 USC 112, second paragraph, examination is carried out assuming "adapted to amplify said signal" means "placed in an environment wherein said signal is amplified" while no amplifying function other than an inherent one as capacitor (through attraction of charges by a control signal on one of its two terminals leading to a larger voltage change on the other terminal) is assumed involved in any adaptation.

*Mead et al teach* (title, abstract, Figures 1, 3, 6, 7, and 9; cols. 2-10) a circuit 10 (col. 2, l. 65) for amplifying signals (abstract, first sentence), the circuit comprising:

a control line (LOAD BIAS connected to a bias voltage source) (cf. col. 3, l. 10-20 and Fig. 7); and

a two terminal semiconductor device 62-1 (MOS transistor used as varactor with source and drain short-circuited: col. 3, l. 33-43; cf. Fig. 1, 9 included as 62-1, 62-2, in Fig. 7), having first and second terminals (loc.cit.), the first terminal (gate of gated diode 62-2) coupled to a signal line 194-1 (of sense amplifier 10), and the second terminal coupled to the control line (capacitively, through 16-1) (loc.cit.), wherein the two terminal semiconductor device is adapted to have a capacitance (gate-channel/source/drain capacitance) when a voltage on the first terminal relative to the second terminal is in a first voltage range and to have a lower capacitance when the voltage on the first terminal relative to the second terminal is in a second voltage range (because the MOS varactor = gated diode inherently has a variable capacitor, wherein the gate voltage can be raised or lowered (depending on the conductivity type of the varactor) to cause depletion, and even further to cause inversion of the channel),

wherein the control line is adapted to be coupled to a control signal (through the capacitive coupling to the aforementioned bias voltage source); and

wherein the signal line is adapted to be coupled to a signal (from the vertical scanner) and to be an output of the circuit (through 218) (col. 8, l. 44-col. 9, l. 64), and wherein the two-terminal semiconductor device is CAPABLE of amplifying said signal in response to a substantial change in voltage of said control signal: by admission by applicant, Figure 11A of disclosure: any amplifying function must be across the node of

1101/1110 and hence is inherent as a property of *capability* of said gate diode. In reference to the claim language referring to ""wherein the two-terminal semiconductor device is adapted to amplify", intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

Finally, the limitation "adapted" pertains itself to a method of making the device and as such constitutes a product-by-process limitation. The limitation "adapted" is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

*On claim 2:* the two terminal semiconductor device by Mead et al comprises a gated diode 62-1 (also 32 in Fig. 1) (Fig. 7) having a well (N.B.:

substrate is a p-well; col. 5, l. 1-5; Fig. 3) because it is implemented as p-type substrate 156 (Fig. 6 and col. 7, l. 65) in Fig. 6, which inherently is a (electrostatic potential) well for all majority charge carriers therein) and wherein the threshold voltage can inherently be modified by modifying a dopant level in said well of the gated diode because said dopant level determines the number of charge carriers (see, for instance, Wolf, ISBN 0-961672-5-3, pages 116-133).

*On claim 9:* the circuit further comprises an output circuit 206-1 / 216 (Fig.7) adapted to produce an output corresponding to a voltage at the gate input of the gated diode (depending as it is on the capacitance of capacitor 62-1).

*On claim 10:* the output circuit comprises one or more of the following: a buffer, an inverter, and a latch, because the hold/sample circuit 206 (col. 9, l. 25-32) is a buffer circuit.

*On claim 13:* the two terminal semiconductor device comprises a gated diode 32 (62-1, 62-2) (col. 3, l. 33-43) (N.B.: source and drain both connected to the output of the sense amplifier and hence also to each other, forming one pole of the diode, the gate forming the other one).

*On claims 14-15:* the gated diode is an n-type gated diode (col. 3, l. 36) or a p-type gated diode (col. 3, l. 33-35), wherein the threshold voltage is a positive, respectively negative voltage (inherently, a positive voltage is required to cause inversion in the former, a negative voltage in the latter, wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal relative to the second terminal is more positive, respectively negative, than the

threshold voltage and to have a lower capacitance when the voltage on the first terminal is less positive, respectively negative, than the threshold voltage.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claim 11*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Mead et al as applied to claim 1, and in view of Ravi et al (US 2004/0263272 A1) and Brachitta et al (6,130,469).As detailed above, Mead et al anticipate claim 1. Mead et al do not teach the further limitation defined by claim 11 as a whole although they clearly teach a MOS n-channel transistor as the basis for their varactor 32, which inherently has an insulation formed between the gate and the well and a source region (see col. 3, l. 33-43), and although they clearly teach the first terminal is coupled to the gate and the second terminal is coupled to the source (see above, discussion of claim 1).

*However, it would have been obvious* to include said further limitation on overlapping of said source region "one side of the insulator and gate" in view of Ravi et al, who teach said overlap in a varactor to be non-zero so as to have a minimum capacitance in the OFF state (see [0066]). *Motivation* to include the teaching by Ravi et al derives from the resulting improved controllability of the ratios of capacitances in OFF and ON state in the varactor so as to have a more accurately quantified varactor.

Furthermore, it would have been obvious to include the limitation "a shallow trench isolation region abutting another side of the insulator and gate" in view of Brachitta et al, who teach said STI region to insulate MOS capacitors from neighboring FET devices (col. 2, l. 13-23) thus making the devices independent as they should. *Motivation* to include the teaching by Brachitta et al in the invention by Mead et al derives from said advantage of device independence coupled with the presence in one wafer of several FETs and the varactor as MOS capacitor also in Mead et al (32 is varactor as MOS capacitor in wafer with FETs (col. 7, l. 3-36).

***Allowable Subject Matter***

2. ***Claims 3-8, 17-20, 24-28, 36 and 37*** are allowed. The following is a statement of reasons for the indication of allowable subject matter: The claimed invention defined by independent claims 3, 24 has not been found in the prior art, nor has said claimed invention been found obvious over the prior art. Reference is also made to the Terminal Disclaimer filed 8/16/07, which has been approved.
3. ***Claim 16*** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: within the context of claim 1 the differential circuit as recited in claim 16 has not been found in the prior art, nor has any prior art been found over which said differential circuit would have been obvious.

***Response to Arguments***

Applicant's arguments filed 8/13/07 have been fully considered but they are not fully persuasive. Although the double patenting rejections of claims 3 and 24 have been withdrawn in light of aforementioned Terminal Disclaimer and although the objection to the Drawings has been withdrawn in light of persuasive Remarks, claims 1-2 and 9-15 still stand as rejected.

In particular,

(a) With regard to the rejection under 35 U.S.C. 112, first paragraph, to "abut" means, according to Merriam-Webster's Collegiate Dictionary, tenth Edition, in the relevant meanings considering the art, only "to touch" or "to border on" (see page 5). As claimed, the source diffusion region and the drain diffusion region both abut and hence touch, or have a common border with, the gate. Because inherently, gate, source diffusion region and drain diffusion region all are conductive, they are all held at substantially the same voltage, and hence no terminal other than the one commonly held by source, drain and gate is in the claimed "two terminal semiconductor device". Therefore, applicants arguments fail to persuade and consequently the rejection under 35 USC 112, first paragraph, of claim 12 stands.

(b) With regard to "Prior Art Rejections", applicant's arguments persist to be based on an allegation for what the device in question is used for (pages 4-5 of Remarks). In other words: applicant persists in arguments against the long-held lack of patentable weight of limitations of intended use. Applicant is referred to the pertinent

portion of the previous office action, page 5, line 17 – page 6, line 2, which is herewith included by reference in its entirety.

Furthermore, even arguendo on intended use, counter to applicant's contention that the varactors of Mead "are not even used for signal amplification", as alleged on page 6 of Remarks, sense amplifier 10 in Mead is used for amplification, while the varactor is comprised in said sense amplifier. This also holds for the use in terms of arrays as depicted in Figure 7 on which the rejection was primarily based. See abstract and col. 8, l. 44+.

On applicant's statement that "Mead does not teach a two-terminal device for performing amplification" exactly the same response is in order: clearly Mead does teach a two-terminal device in the form of the varactor 62-1 (shown in a single unit as 32 within sense amplifier 10), and hence the only question on applicant's statement quoted above is whether said varactor is capable of amplification. It is so capable because sense amplifier 10 in Mead is used for amplification, while the varactor is comprised in said sense amplifier. This also holds for the use in terms of arrays as depicted in Figure 7 on which the rejection was primarily based. See abstract and col. 8, l. 44+.

Applicant's argument (remainder of page 6 of Remarks) that Mead does not teach an amplification control line fails to persuade, because the second terminal connects capacitively to 16-1, which a load bias controls through transistor 16-1. That the connection is *not direct*, as contended by applicant, is not claimed and hence is irrelevant. Therefore, applicant's argument is not persuasive.

Once again, on applicant's arguments on page 7, that "the varactor is not adapted to amplify a signal" is as such neither claimed nor does it carry patentable weight in the presence of the capability, the capability having been shown and discussed in the foregoing portion of this response. The argument by applicant on coupling element has already been discussed overleaf. That the varactor is an integral part of a sense amplifier and is hence used for amplification is evident from the quoted portions of Mead. That Mead does not disclose or suggest a coupling element coupled to a control line and a control signal is demonstrably incorrect in light of the above-included discussion of the capacitive coupling to 16-1 controlled by a gate connected directly to a load bias, as discussed overhead in response to applicant's allegation that a direct coupling is absent; however, the claim language does not recited any direct coupling, even when interpreted as non-capacitive (note that there is little that is indirect about a coupling through a capacitance). Finally on this section, that the LOAD BIAS signal is a DC voltage and hence cannot be a control signal, as suggested by applicant, is incorrect, because even the voltage in a DC signal can be varied so as to control the load transistor 16-1 capacitively (through its gate voltage).

On Applicant's Response to "Response to Arguments", first paragraph, applicant refers to Appeal Brief, which examiner does not find in the file. Furthermore, the varactor by Mead et al certainly qualities as a two-terminal device, one being the source/drain terminal, the other terminal being the gate. The repeat of applicant's arguments on LOAD BIAS are herewith responded to in exactly the same manner through inclusion of the aforementioned comments by reference in their entirety.

Especially unpersuasive is the notion advanced by applicant that simply because a voltage is DC it cannot be used for amplification. Any gate with a DC voltage still has control over the source/drain current through variation of the magnitude of the DC voltage.

In light of the above comments applicant's arguments are not deemed persuasive and hence the rejections over Mead et al stand, previous rejections having been included without any change intended.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
October 25, 2007

Primary Patent Examiner:
Johannes Mondt (TC3600, Art Unit: 3663)